FIG. 1

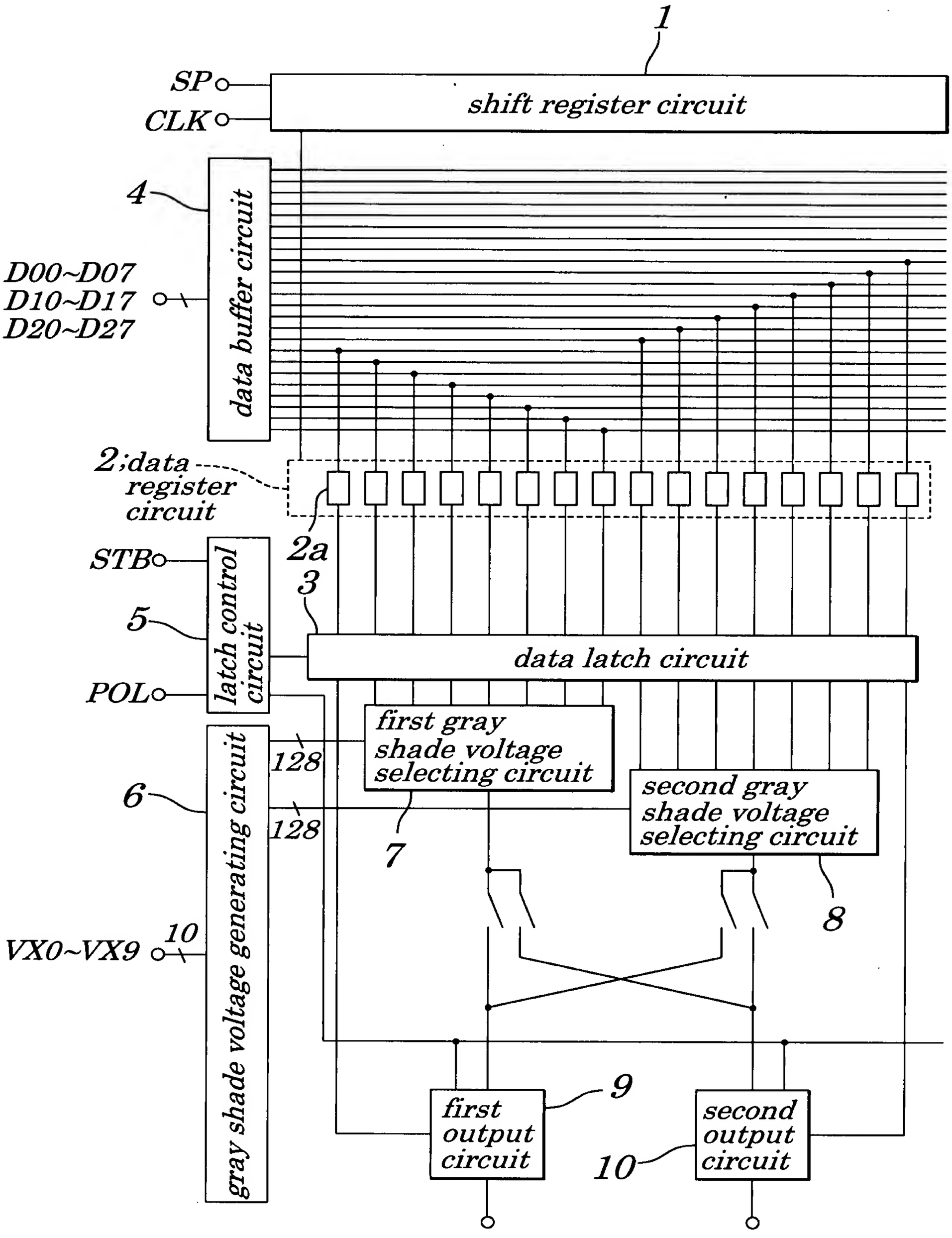
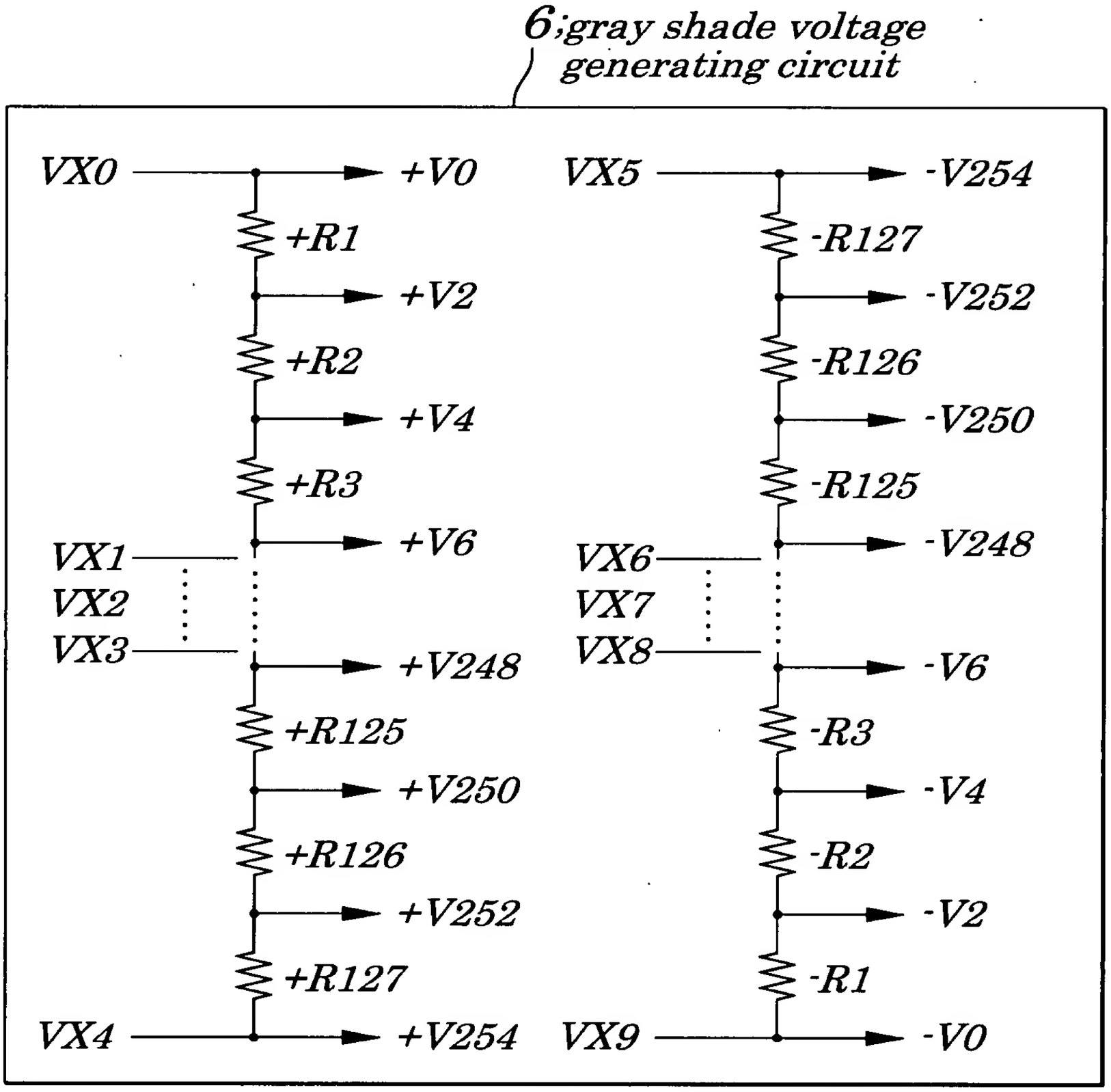

1
SP
CLK
shift register circuit
4
data buffer circuit
D00~D07
D10~D17
D20~D27
2;data register circuit
2a
3
STB
5
latch control circuit
POL
data latch circuit
first gray shade voltage selecting circuit
second gray shade voltage selecting circuit
128
128
6
7
8
gray shade voltage generating circuit
VX0~VX9
10
first output circuit
9
second output circuit
10

FIG.2


6;gray shade voltage generating circuit
VX0
+V0
+R1
+V2
+R2
+V4
+R3
+V6
VX1
VX2
VX3
+V248
+R125
+V250
+R126
+V252
+R127
VX4
+V254
VX5
-V254
-R127
-V252
-R126
-V250
-R125
VX6
-V248
VX7
VX8
-V6
-R3
-V4
-R2
-V2
-R1
VX9
-V0

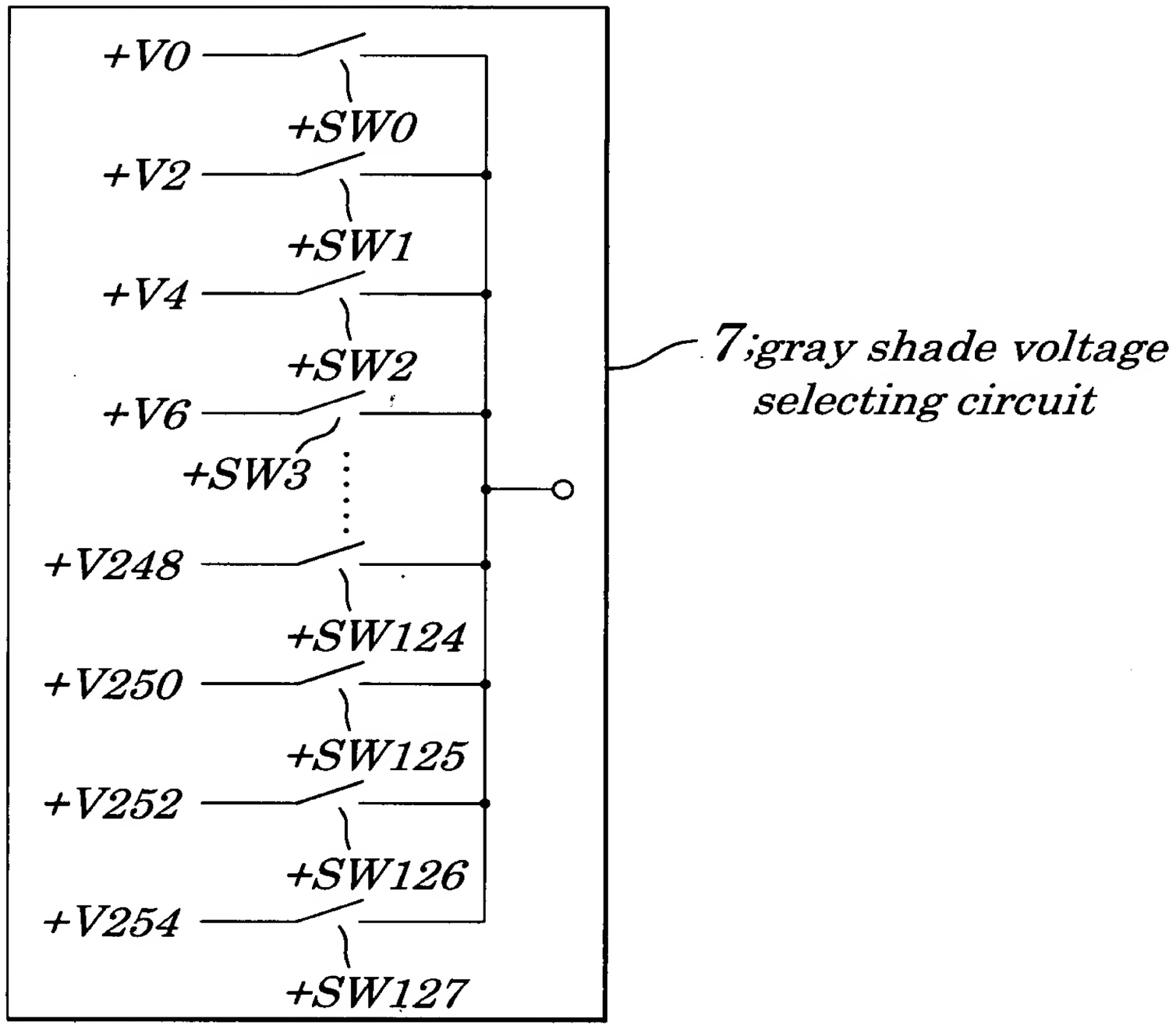

+V0
+SW0
+V2
+SW1
+V4
+SW2
+V6
+SW3
+V248
+SW124
+V250
+SW125
+V252
+SW126
+V254
+SW127
7;gray shade voltage selecting circuit

FIG.3A

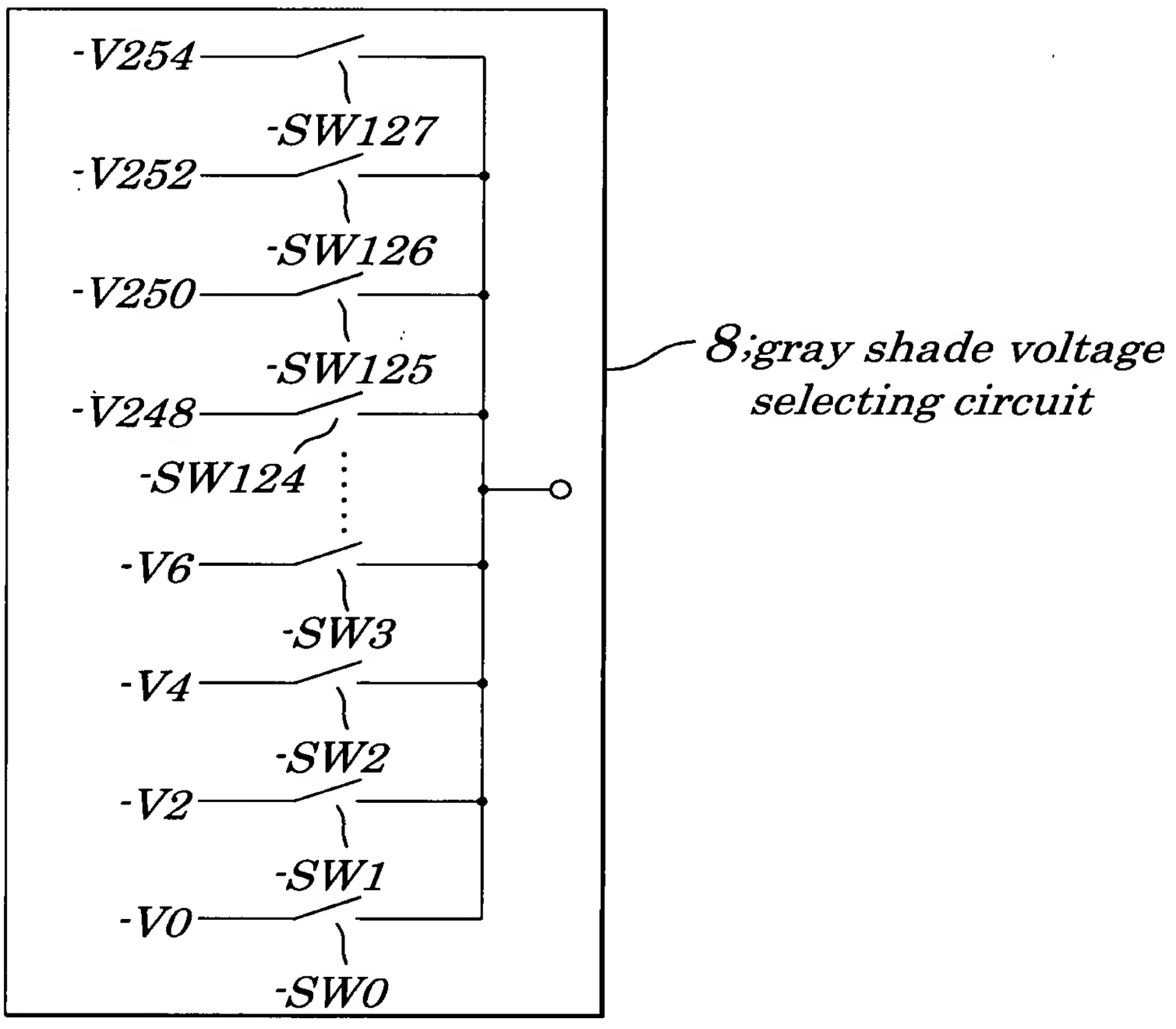

-V254
-SW127
-V252
-SW126
-V250
-SW125
-V248
-SW124
-V6
-SW3
-V4
-SW2
-V2
-SW1
-V0
-SW0
8;gray shade voltage selecting circuit

FIG.3B

FIG.4

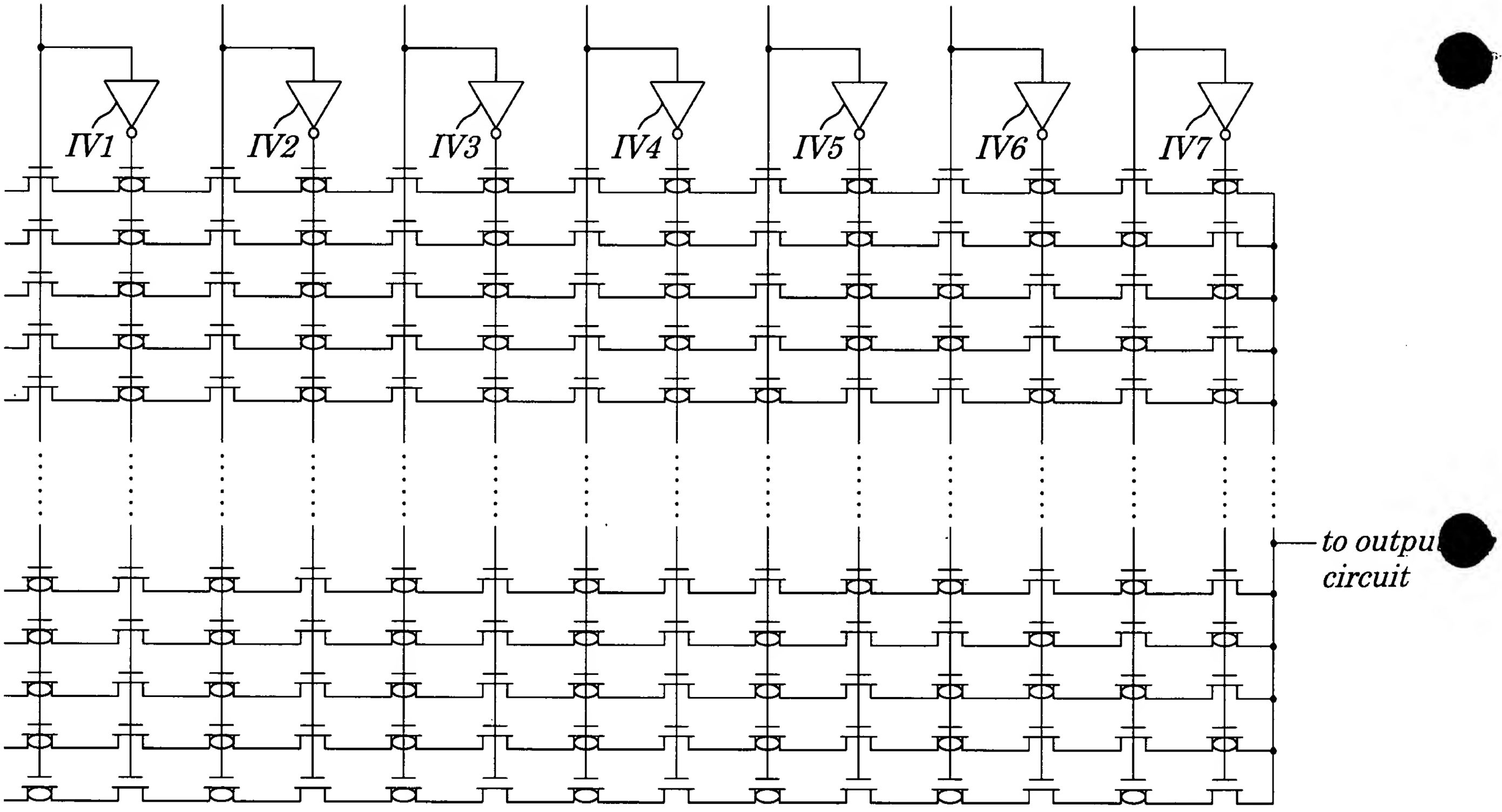

from data latch circuit
IV1
IV2
IV3
IV4
IV5
IV6
IV7
to output circuit

FIG.5

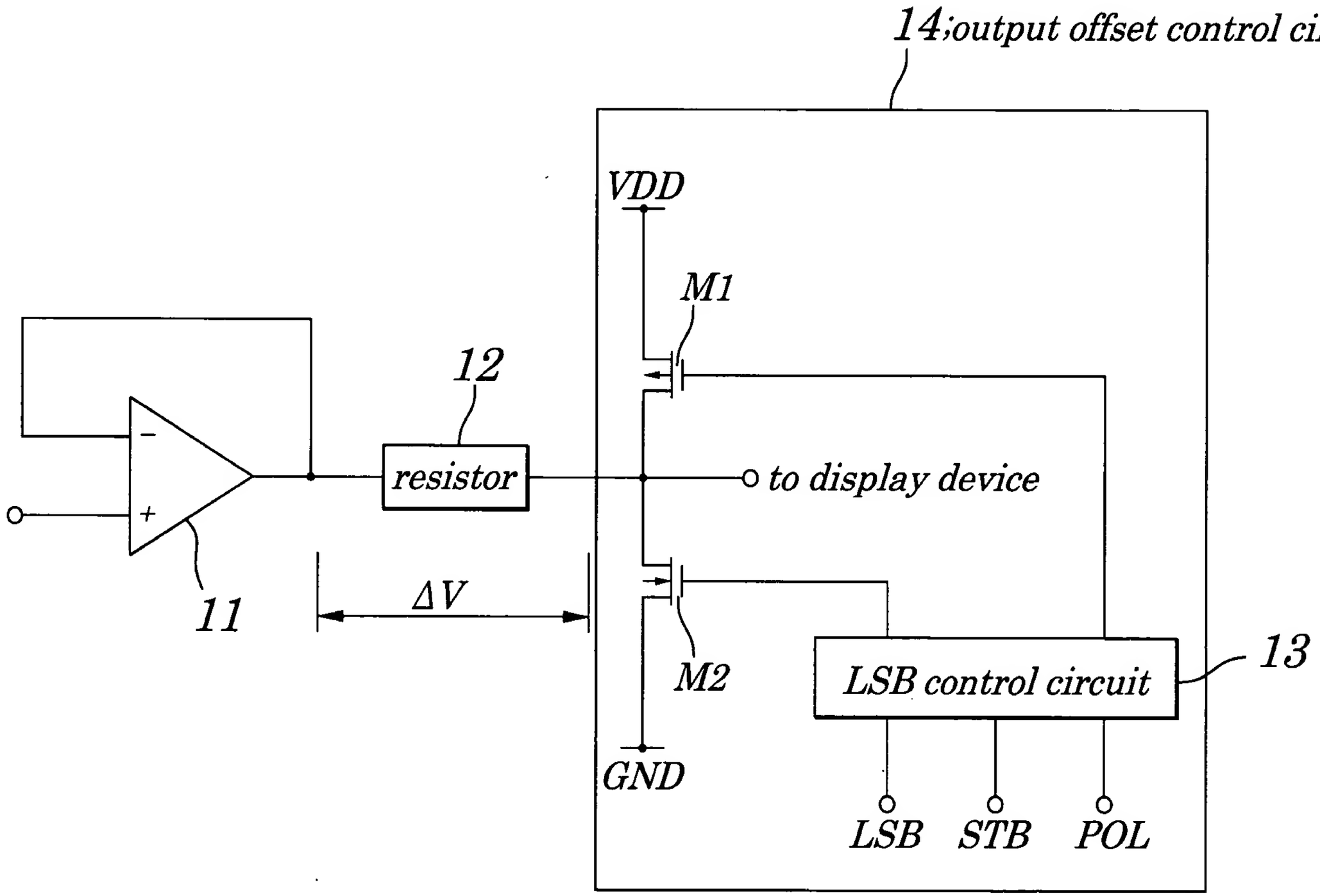

14;output offset control circuit
VDD
M1
12
resistor
to display device
11
ΔV
M2
LSB control circuit
13
GND
LSB
STB
POL

FIG.6

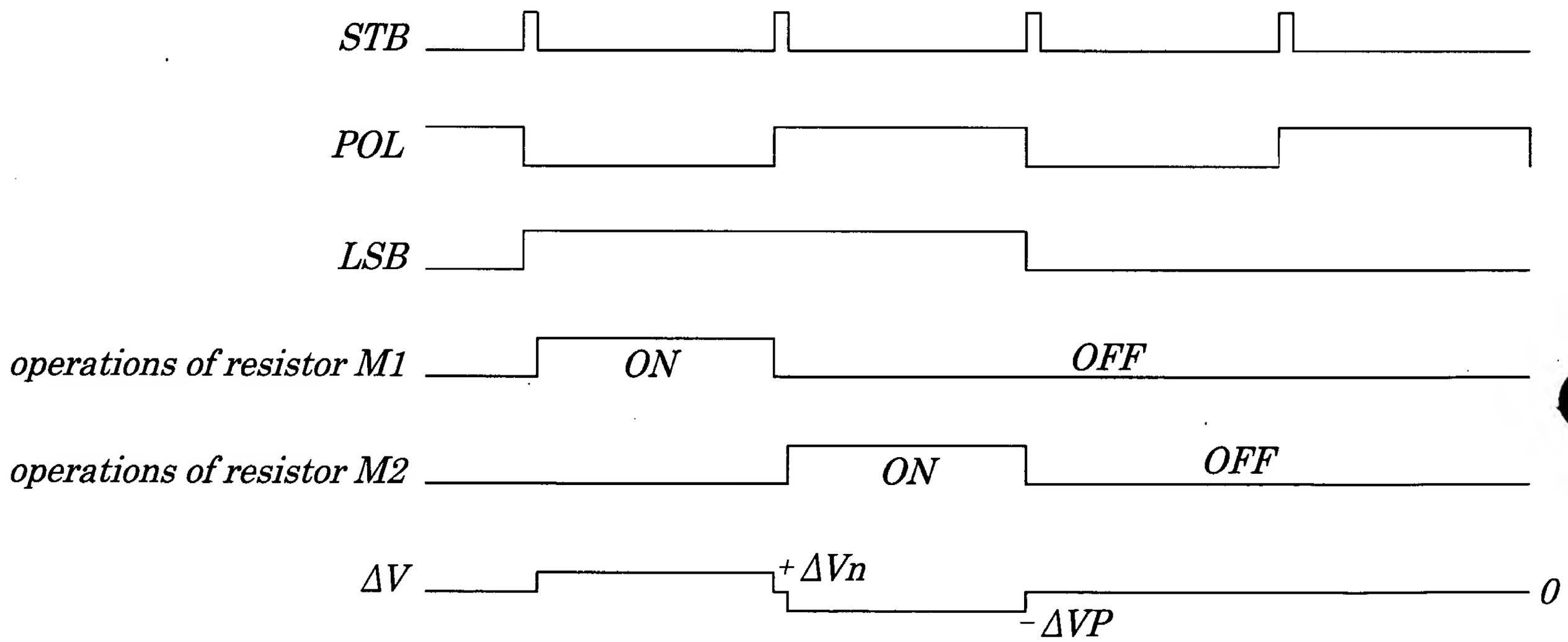

STB
POL
LSB
operations of resistor M1
ON
OFF
operations of resistor M2
ON
OFF
ΔV
+ΔVn
0
−ΔVP

FIG. 7

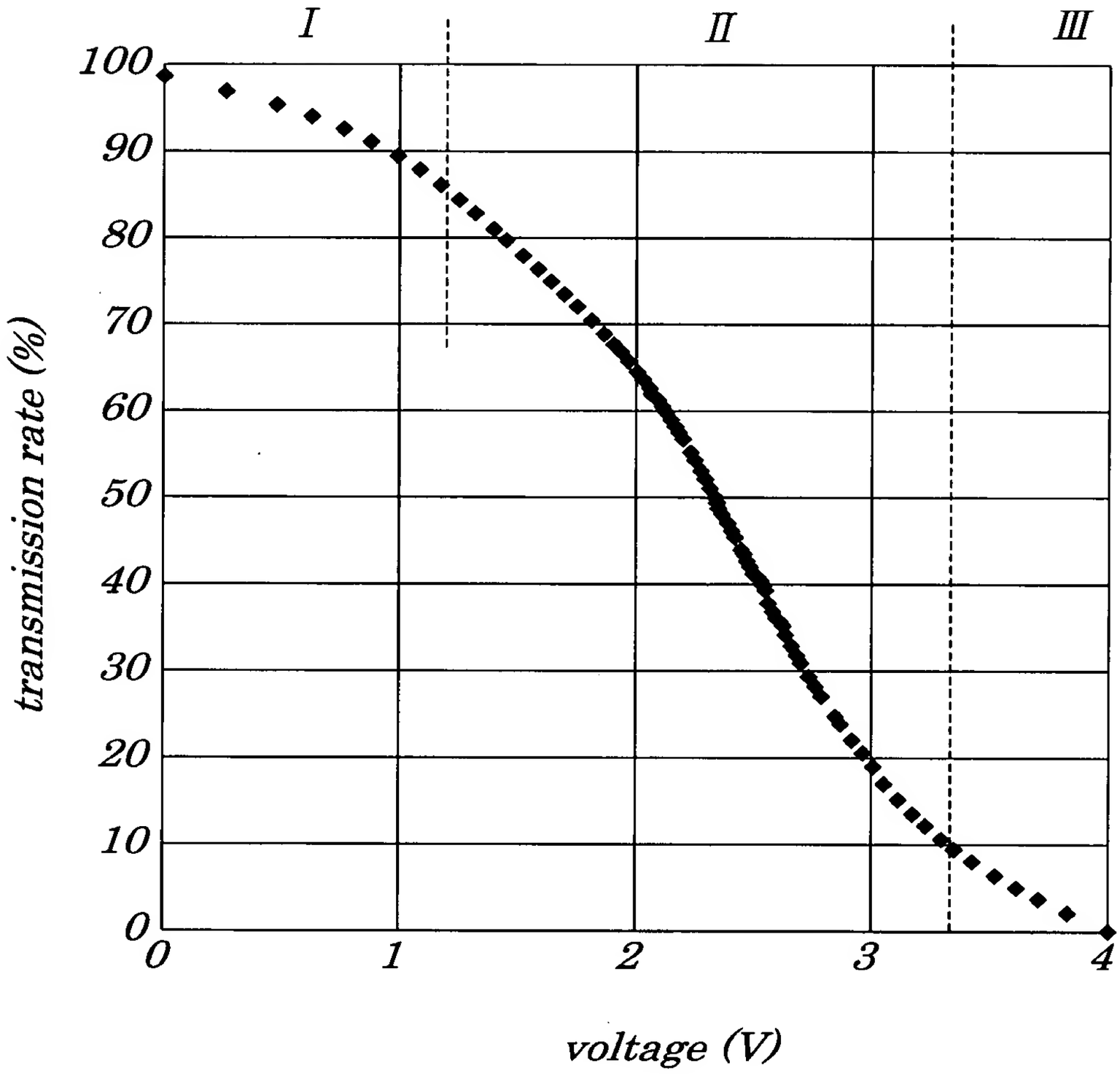

I
II
III
100
90
80
70
60
50
40
30
20
10
0
0
1
2
3
4
transmission rate (%)
voltage (V)

FIG.8A

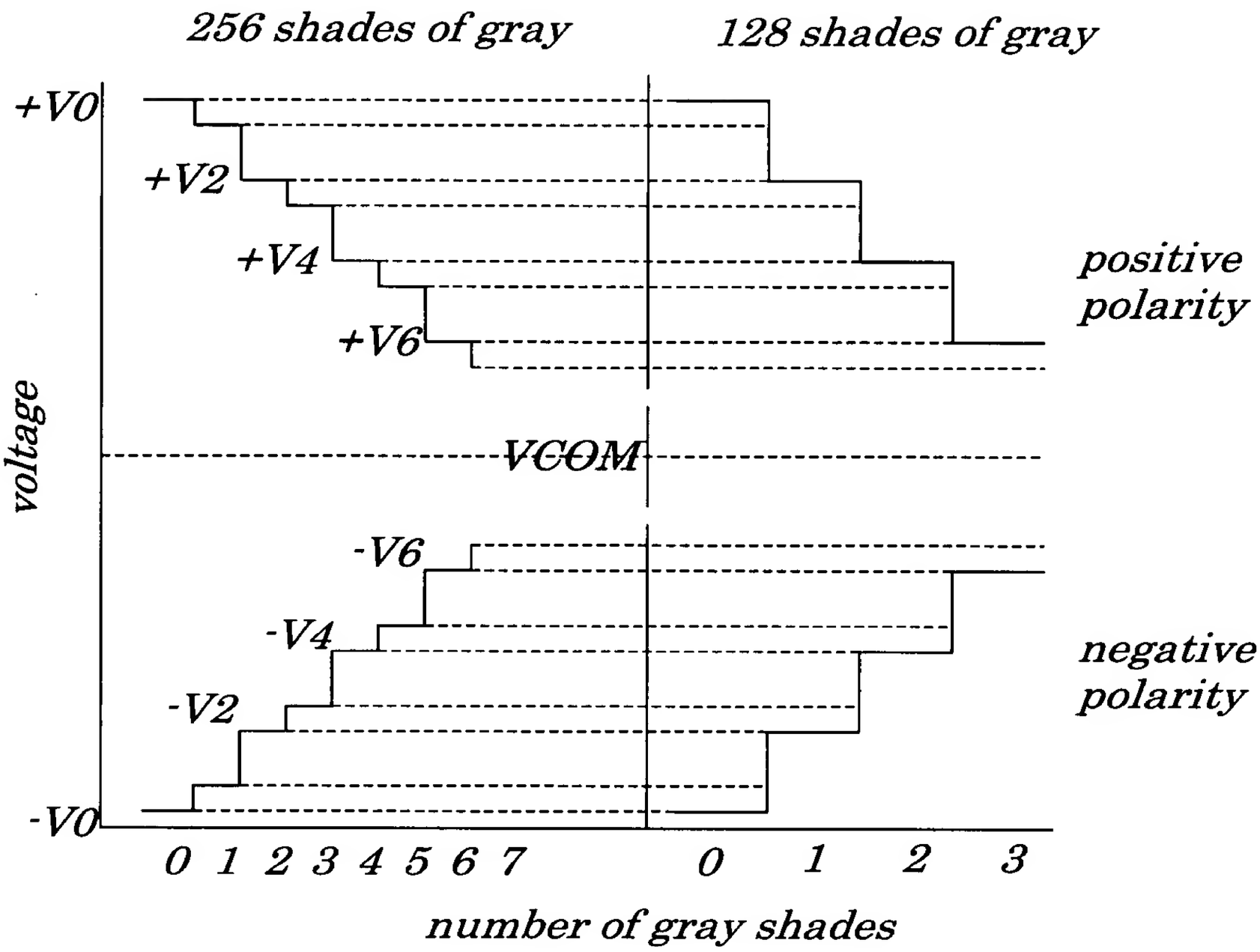

256 shades of gray
128 shades of gray
+V0
+V2
+V4
+V6
positive polarity
VCOM
-V6
-V4
-V2
-V0
negative polarity
voltage
0 1 2 3 4 5 6 7
0 1 2 3
number of gray shades

FIG.8B

256 shades of gray
128 shades of gray
+V126
+V128
+V130
+V132
VCOM
-V132
-V130
-V128
-V126
positive polarity
negative polarity
voltage
126 128 130 132
127 129 131 133
63 64 65 66
number of gray shades

FIG.9

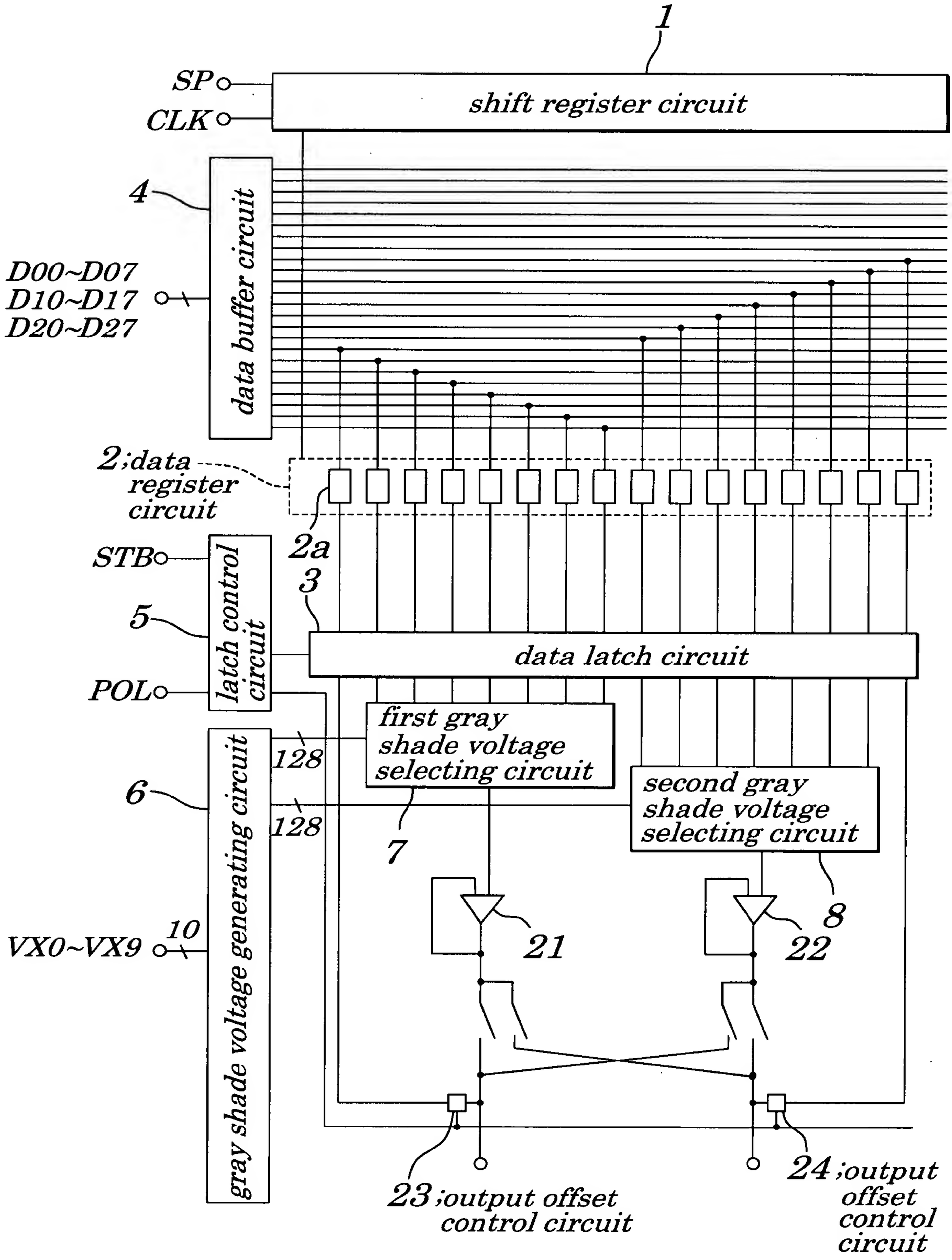

1
SP
CLK
shift register circuit
4
data buffer circuit
D00~D07
D10~D17
D20~D27
2;data register circuit
2a
3
STB
5
latch control circuit
POL
data latch circuit
first gray shade voltage selecting circuit
second gray shade voltage selecting circuit
128
128
6
7
8
21
22
10
VX0~VX9
gray shade voltage generating circuit
23;output offset control circuit
24;output offset control circuit

FIG.10

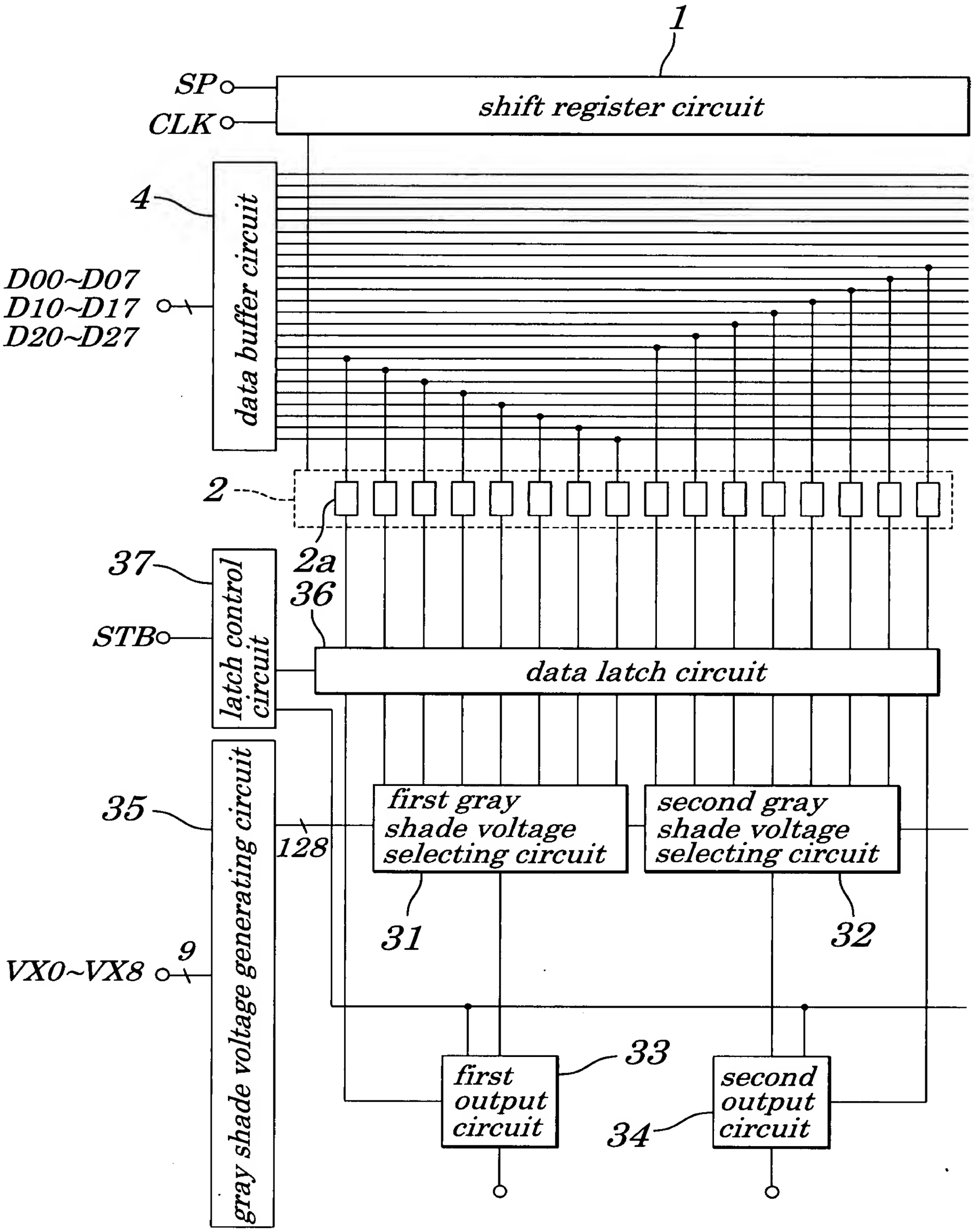

1
SP
CLK
shift register circuit
4
data buffer circuit
D00~D07
D10~D17
D20~D27
2
2a
36
37
STB
latch control circuit
data latch circuit
35
gray shade voltage generating circuit
128
first gray shade voltage selecting circuit
second gray shade voltage selecting circuit
31
32
VX0~VX8
9
33
first output circuit
34
second output circuit

FIG.11 (PRIOR ART)